

CDEによる受託加工サービスのご説明

Contracted Processing Service by CDE (Chemical Dry Etcher)

SHIBAURA MECHATRONICS CORPORATION
Fine Mechatronics Division

Contents

■ Introduction

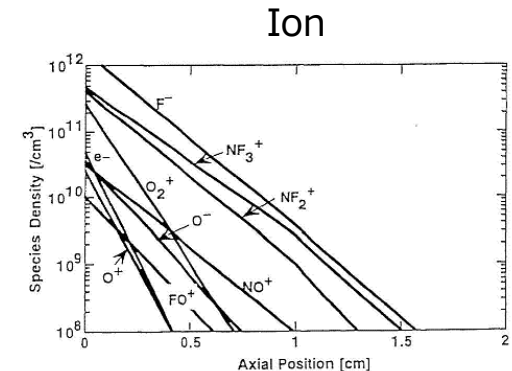
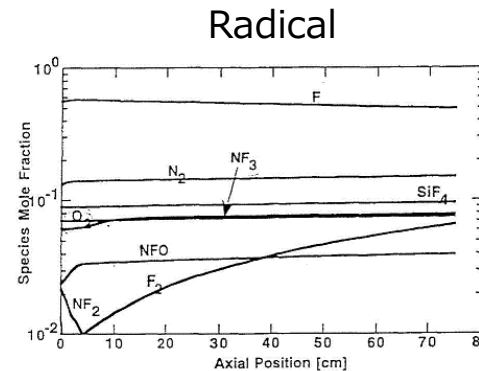
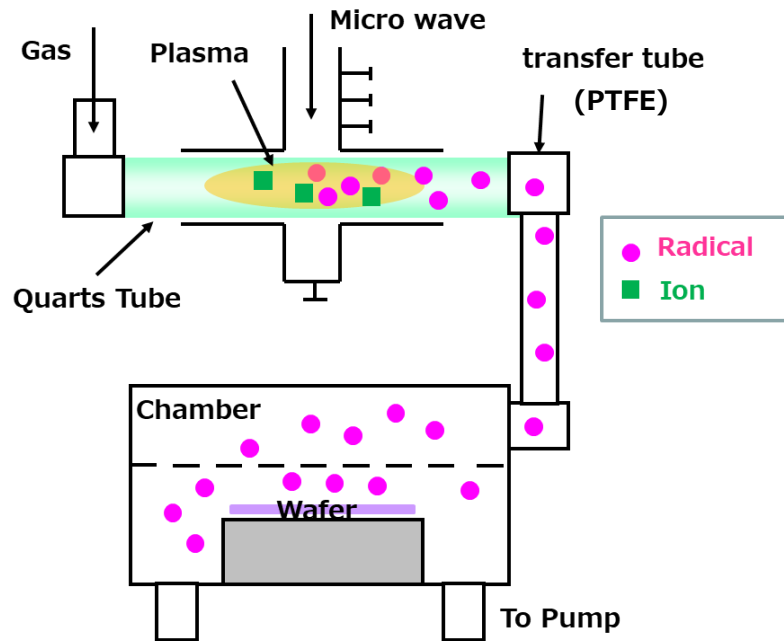
- ✓ **CDE Feature ~ Why User needs CDE System**
- ✓ **Example of CDE Result**

■ Contracted Processing Service

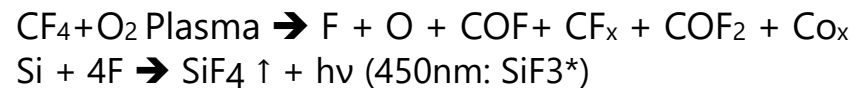
- ✓ **Procedure**
- ✓ **Tools and Specification**
- ✓ **Process Application and Material**

Feature (Chemical Dry Etcher)

Isotropic Etching and Plasma Damage Free



Reference : E.Meeks他 "Result from modeling and simulation of CDE systems," Sandia National Laboratories Report SAND96-8241



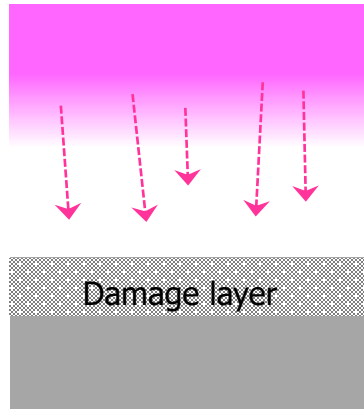
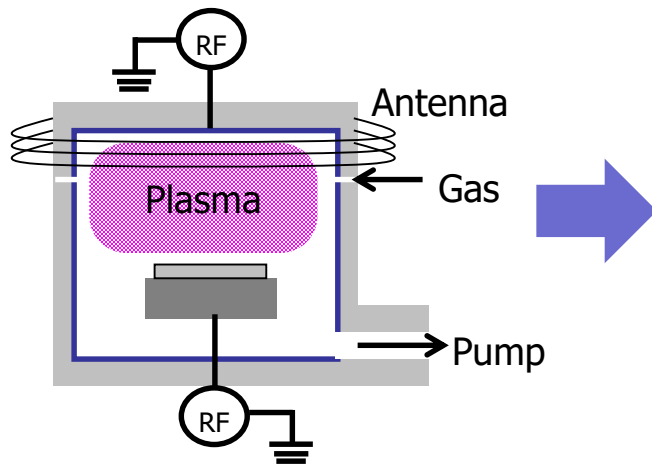
CDE (Remote Plasma) provides...

- ✓ Isotropic Etching
- ✓ Plasma Damage Free Etching (much better than ICP/CCP Plasma)
- ✓ Device Performance Improvement

Why user needs CDE system

Shibaura's CDE (Chemical Dry Etching) technology provides Plasma Damage Free !!

ICP/RIE (Plasma in Chamber)

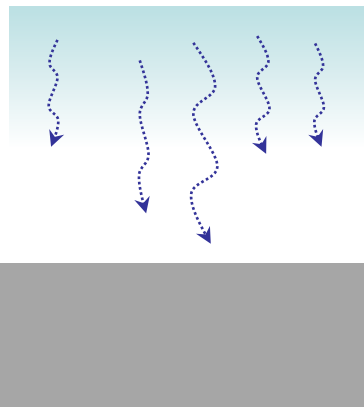
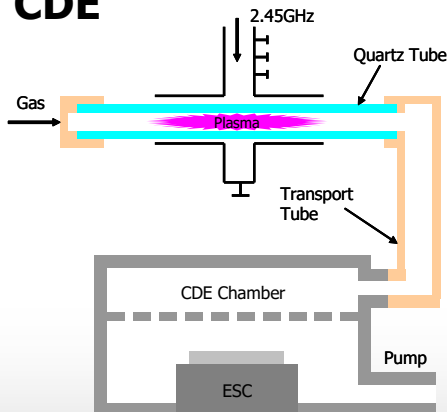


Ion damage !!
Ion Charge !!

ICP/RIE process,
plasma damage occurs at surface.

→ Device characteristics deteriorate.
(Customer information)

CDE

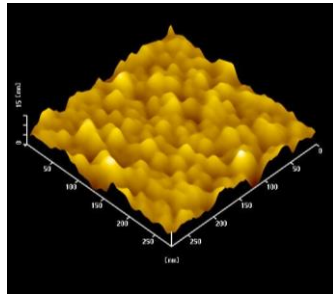


Only radical !! → Isotropic Etch
Ion Free !!
No Ion Charge !!

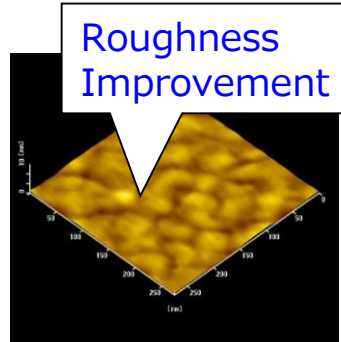
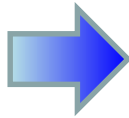
CDE process,
plasma damage dose not occur at
surface.

Example of CDE Result

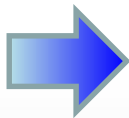
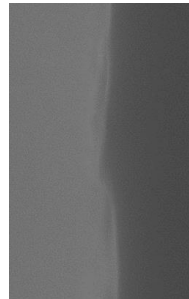
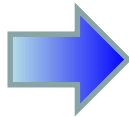
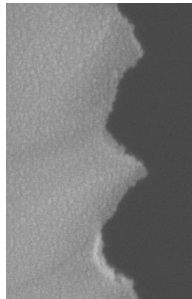
■ Si Surface Smoothing



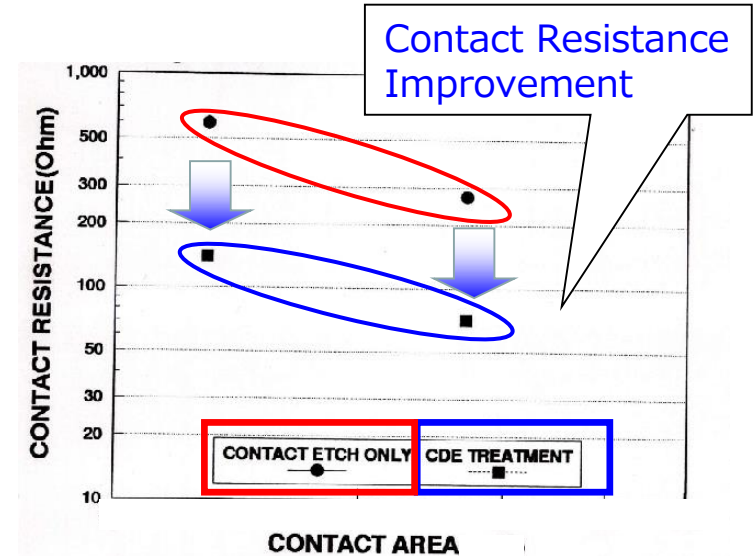
Ra: 1.24nm



Ra: 0.17nm



■ Si Damaged Layer Removal



Contents

■ Introduction

- ✓ CDE Feature ~ Why User needs CDE System
- ✓ Example of CDE Result

■ Contracted Processing Service

- ✓ Procedure
- ✓ Tools and Specification
- ✓ Process Application and Material

Service Procedure

1. 評価内容・試作のご相談

Discussion for Contracted Processing



- ・プロセスエンジニアとのお打合せ ⇒ 評価内容についてお取決め
Discussion with process engineer
Considering the evaluation plan
- ・御見積価格のご連絡 ⇒ ご評価内容を決定
Sending the quotation
Fix the evaluation items/procedure

2. 条件出し、ご評価

Evaluation by SHIBAURA



- ・条件出し評価、試作評価の実施 ⇒ デモ機見学、お立合い出来ます
Executing the best evaluation
Demo Tool Tours in our fab (If you want)

3. 評価ご報告、今後の進め方ご相談

Evaluation Report and Discussion for the next step

- ・報告書の作成、ご報告 ⇒ 費用のお支払い
Sending the report
Acceptance and payment
- ・今後の進め方ご相談 ⇒ CDE受託加工の継続等について
Discussion for the next step
Discussion for the next step

Evaluation Tools

Our Clean Room (Class 10)

Process Tools



CDE-80
(3~8inch)



* CDE300
(12inch)

* ICE200/300
[ICP+Bias]
[Low Temp]
[Ashing]
(8-12inch)



* Single WET
(12inch)



* Draft Chamber (Fumehood)
(for batch WET by coupons)

* Sub-Tools for Unit Process: need to discuss for use

Analysis Tools

- 光学顕微鏡 (Optical Microscope)
- 膜厚測定器 (Thickness Measurement)
- 電子顕微鏡 (SEM)
- エネルギー分散型X線分析 (EDX)
- 段差測定器 (Step Height Measurement)
- 蛍光X線 (X-ray fluorescence spectrometers)
- パーティクル測定器 (Particle Detector)
- オシロスコープ (Oscilloscope)
- サーモグラフィカメラ (Thermography Camera)
- 接触角計 (Contact angle meter)
- XPS, ToF-SIMS, AES, AFM, IC-Mass etc, the other analysis tools are outsourcing

Service Specification

<p>Service Summary</p>	<ul style="list-style-type: none"> • Isotropic Chemical Dry Etching by CDE-80 • Plasma Damage Free (Remote Plasma) • Discussion for Evaluation (Item, procedure, schedule etc) • On-site Analyze (Microscope, Particle, Thickness, SEM/EDX) • Outsourcing Analyze (XPS, AFM, TEM, AES, ToF-SIMS etc) • Unit Process Support by using the outer tools (※TDB: WET Draft Chamber, Single WET Processor, Ashing) • Demo tool tours in our fab
<p>Specification</p>	<ul style="list-style-type: none"> • Plasma : Remote Plasma by micro wave (2.45GHz) • Gas : CF₄, O₂, N₂, Cl₂, NF₃, SF₆, CH₂F₂, H₂/N₂, Ar, He • Stage Temp. : 15~120℃ (※~350℃ by special demo tool) • Sample Size : 6inch/8inch(/12inch by CDE300) SEMI wafer Maximum : $r \leq 300\text{mm}$, Height $\leq 50\text{mm}$ Minimum : about 10mm square (coupon process)

Process Application

Material	<ul style="list-style-type: none"> • General : Si, Si₃N₄, SiO₂, Resist, SiGe • Metal : Ti, TiN, W, Ta, TaN, Mo, Cr, Ru etc • The others : SiC, GaN, Ga₂O₃ • Special : Glass, Films, Thin wafer, TDB for the others • Surface Modification : AL, AL₂O₃, Cu, Au, Ag, Co, Ni, In, Sn, Zn etc
Process Application	<ul style="list-style-type: none"> • Damaged Layer Removal (Light Etching) • Surface Roughness Smoothing • Corner Rounding • Etch Back / Recess • Removal (high selectivity removal) • Surface Modification • Residue Removal (De-Scum)

どんなことでもお気軽にお問合せください。

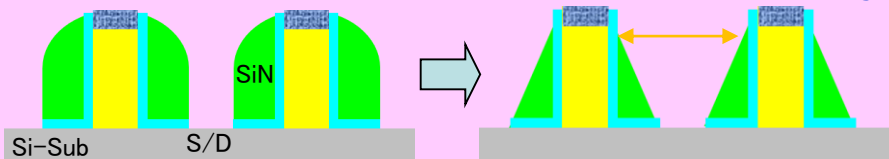
If you have any question/interesting, please let us know.

CDE Process Applications

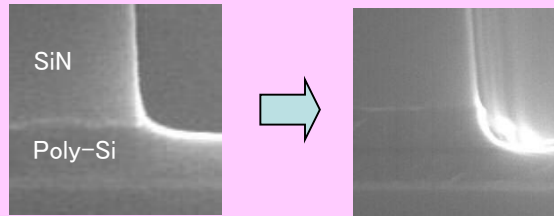
Device Improvement Process

Logic / Flash

Spacer SiN Pull Back



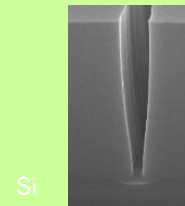
Poly/SiN Selectivity=1 Taper Etching



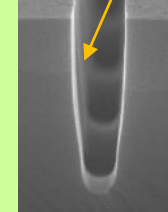
Yield Improvement

CMOS Image Sensor

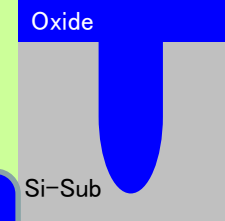
STI Damage Removal



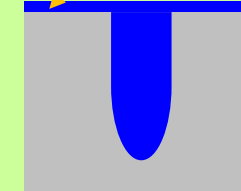
Si Surface No Plasma Damage



Oxide Etch Back



Si Interface
No Plasma Damage



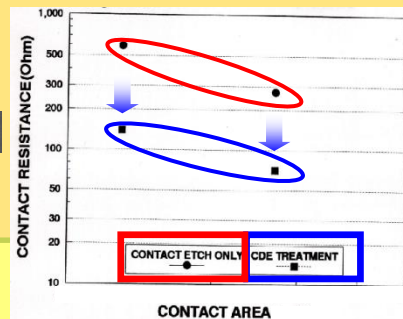
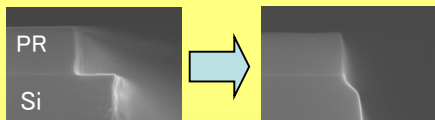
Improvement White Spot, Dark Current

Power Device/Discrete

Si Contact Damage Removal



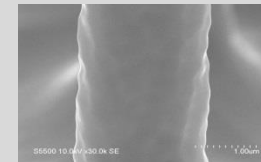
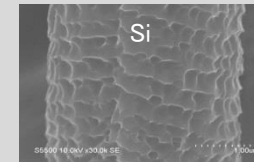
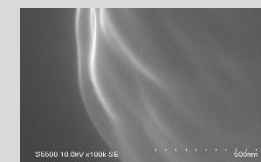
Corner Rounding



Improvement Contact Resistance and E-Mobility

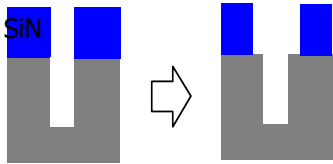
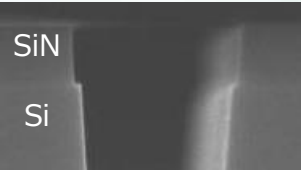
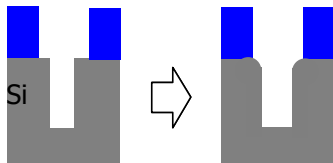

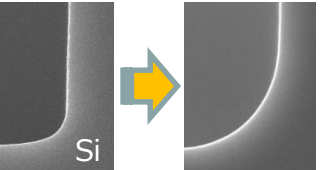
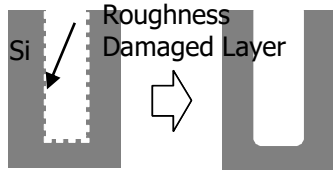
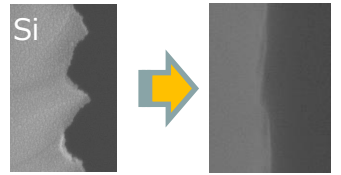
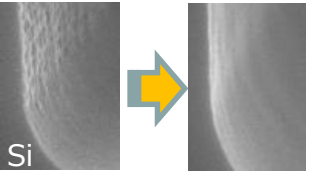
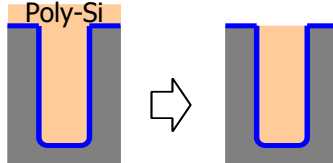

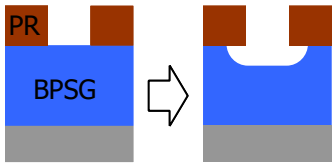
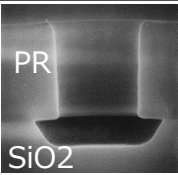
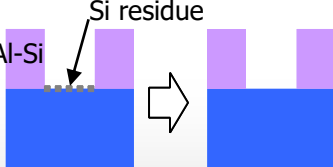


TSV / MEMS

Scallop Smoothing

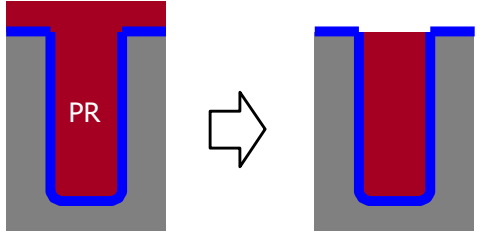
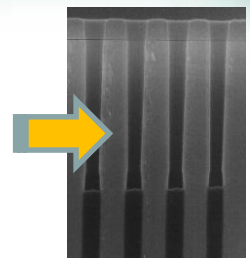
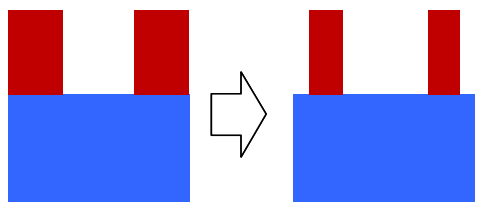
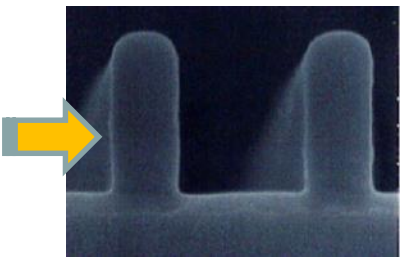
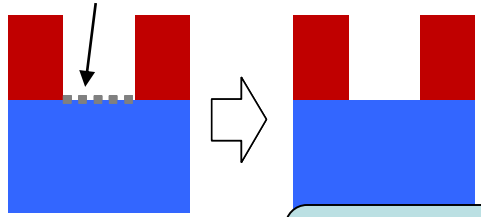

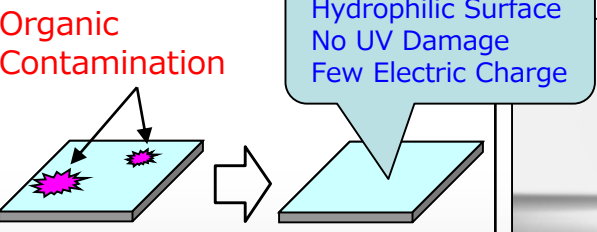
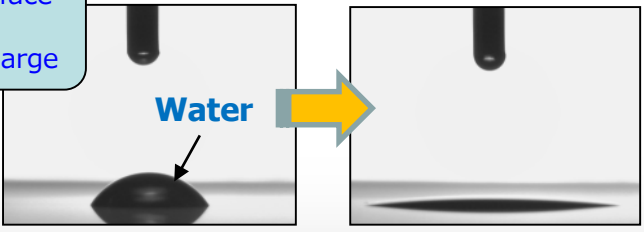


Improvement Film Cruck and Particle

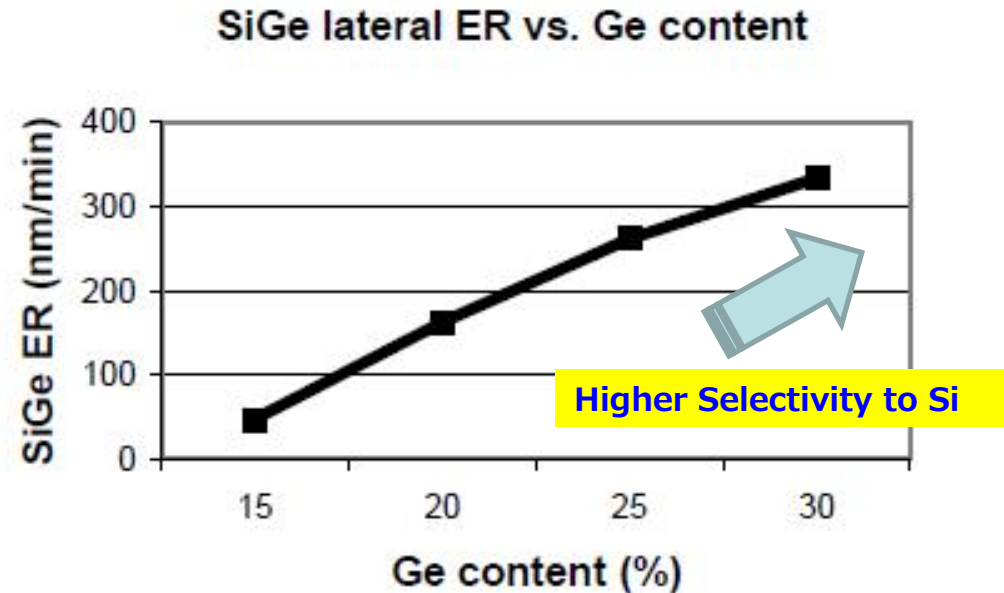
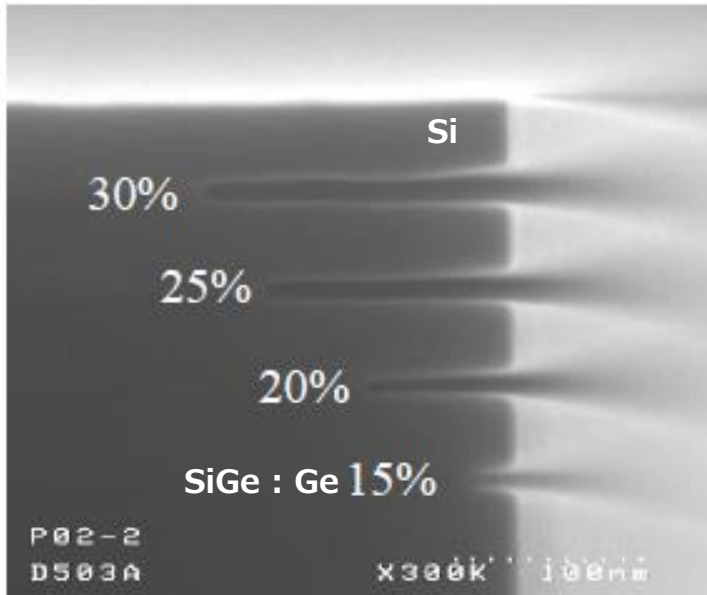
CDE Si Material Process Table

No.	Process	Sketch	Picture
(1)	SiN Pull Back		
(2)	Si Corner Rounding		 
(3)	Si smoothing Damaged Layer Removal		 
(4)	Poly-Si Etch back		
(5)	BPSG Round Etch		
(6)	After Al-Si etch Si residue remove		 

CDE Resist Process Application

No.	Process	Resist E/R	Sketch	Picture
(1)	Recess (Etch Back)	300~1700 [nm/min]		
(2)	Sliming	5~100 [nm/min]		
(3)	Descum	~1700 [nm/min]		
(4)	Surface Cleaning (Hydrophobic → Hydrophilic)	~10 [nm/min]		

Fundamental Data for SiGe



ECS 2006

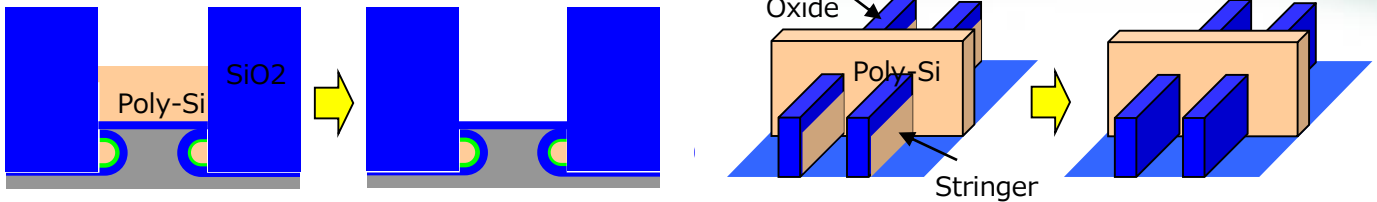
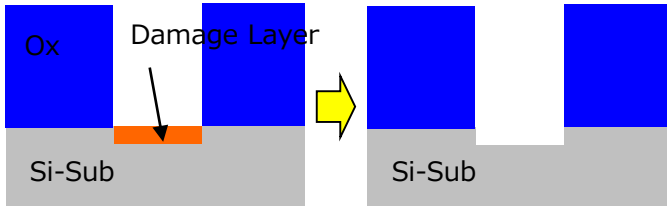
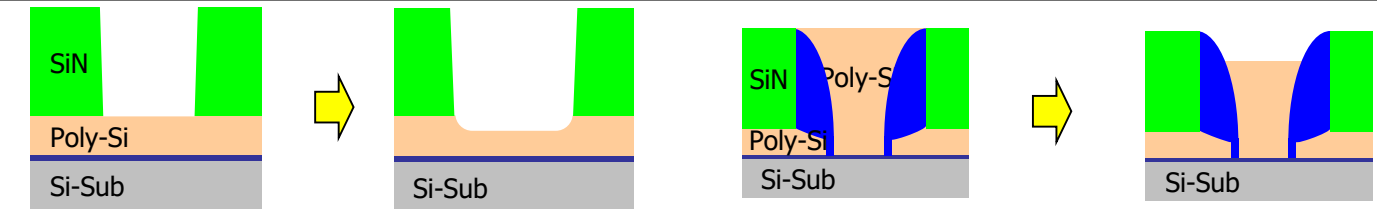
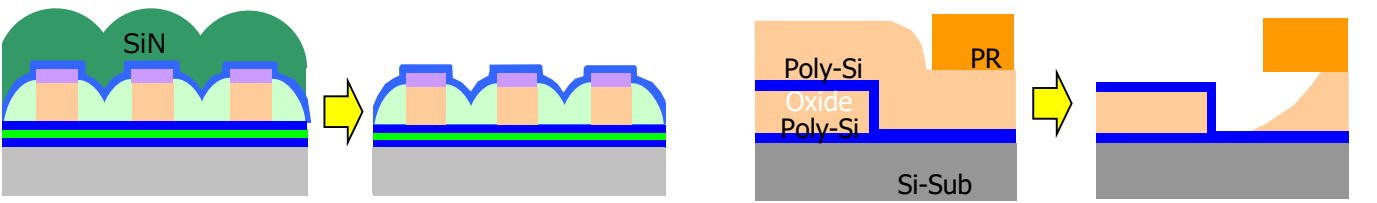
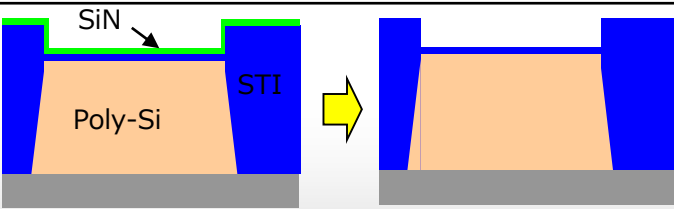
Isotropic Etching of $\text{Si}_{1-x}\text{Ge}_x$ Buried Layers Selectively to Si for the Realization of Advanced Devices.

S. Borel, V. Caubet, J. Bilde, A. Cherif, C. Arvet, C. Vizioz, J.M.Hartmann, G. Rabillé, T. Billon

ECS Transactions - Cancun" Volume 3, "SiGe and Ge: Materials, Processing, and Devices"

High Ge Concentration will achieve higher SiGe/Si selectivity

CDE Memory Process

Process Type	
Poly-Si Removal	 <p>The diagram shows two stages of Poly-Si removal. In the first stage, a cross-section shows a blue Poly-Si layer on a grey Si-Substrate, with a yellow SiO2 layer on top. A yellow arrow points to the second stage, where the Poly-Si layer has been removed, leaving a gap. In the second stage, a 3D view shows a blue Poly-Si layer on a grey Si-Substrate, with a yellow SiO2 layer on top. A yellow arrow points to the final stage, where the Poly-Si layer has been removed, leaving a gap. Labels include 'Oxide', 'Poly-Si', and 'Stringer'.</p>
Damaged Si Removal	 <p>The diagram shows two stages of Damaged Si removal. In the first stage, a cross-section shows a blue Ox layer on a grey Si-Substrate, with a red Damage Layer on top. A yellow arrow points to the second stage, where the Damage Layer has been removed, leaving a gap. Labels include 'Ox' and 'Si-Sub'.</p>
Etch Back (SiN, Poly-Si)	 <p>The diagram shows two stages of Etch Back. In the first stage, a cross-section shows a green SiN layer on a grey Si-Substrate, with a yellow Poly-Si layer on top. A yellow arrow points to the second stage, where the Poly-Si layer has been etched back, leaving a gap. In the second stage, a 3D view shows a green SiN layer on a grey Si-Substrate, with a yellow Poly-Si layer on top. A yellow arrow points to the final stage, where the Poly-Si layer has been etched back, leaving a gap. Labels include 'SiN', 'Poly-Si', and 'Si-Sub'.</p>
Removal (SiN, Poly-Si)	 <p>The diagram shows two stages of Removal. In the first stage, a cross-section shows a green SiN layer on a grey Si-Substrate, with a yellow Poly-Si layer on top. A yellow arrow points to the second stage, where the Poly-Si layer has been removed, leaving a gap. In the second stage, a 3D view shows a green SiN layer on a grey Si-Substrate, with a yellow Poly-Si layer on top. A yellow arrow points to the final stage, where the Poly-Si layer has been removed, leaving a gap. Labels include 'SiN', 'Poly-Si', 'Oxide', 'Poly-Si', and 'Si-Sub'.</p>
ONO SiN Etching	 <p>The diagram shows two stages of ONO SiN Etching. In the first stage, a cross-section shows a blue SiN layer on a grey Si-Substrate, with a yellow Poly-Si layer on top. A yellow arrow points to the second stage, where the Poly-Si layer has been etched back, leaving a gap. Labels include 'SiN', 'Poly-Si', and 'STI'.</p>

CDE Process Capability Table

Etch Material	Main Process	Temp. [deg]	Etch Rate [nm/min]	Unif. [%]	Selectivity		
					Poly-Si	Ox	SiN
Poly-Si	Recess / Etch Back / Removal	15~120	30 ~ 500	<±3		10~100	10~30
	Damaged Layer Removal / Smoothing / Rounding	25~120	3 ~ 30	<±4		1~20	0.2~10
SiN	Etch Back / Removal	25	30 ~ 100	<±4	1~20	10~100	
	Pull Back /	25	3 ~ 30	<±5	0.2~10	1~20	
Ox	Etch Back / Round Etch	70~120	5 ~ 100	<±5	< 1		< 2
Metal	Etch Back (W, Mo)	25~120	200 ~ 300	<±10	No data		< 6
PR	Removal / Recess	70~100	100 ~ 2000	<±5	No data	> 100	> 100
	Residue Strip / Sliming / Descum	25~100	30 ~ 100	<±5	No data	10~100	10~100

END